In the Claims:

1 (withdrawn). A semiconductor configuration, comprising:

a base layer made of semiconductor material;

an insulation layer arranged above said base layer;

a monocrystalline silicon layer disposed above and adjoining said insulation layer, said monocrystalline silicon layer and said insulation layer forming an interface therebetween; and

a passivating substance X forming Si-X bonds at said interface between said insulation layer and said monocrystalline silicon layer, whereby a bond energy of one of said Si-X bonds is greater than a bond energy of an Si-H bond.

2 (withdrawn). The semiconductor configuration according to claim 1, wherein said base layer is a semiconductor substrate.

3 (withdrawn). The semiconductor configuration according to claim 1, wherein said passivating substance X is a substance selected from the group consisting of halogen and nitrogen.

4 (withdrawn). The semiconductor configuration according to claim 1, which further comprises:

a plurality of laterally adjacent, differently doped regions formed in said monocrystalline silicon layer, said regions forming a source region, a channel region, and a drain region of a MOSFET; and

a gate oxide layer disposed above said channel region and an electrical connection structure forming a gate of the MOSFET disposed on said gate oxide layer.

5 (withdrawn). The semiconductor configuration according to claim 4, wherein said channel region in said monocrystalline silicon layer and said gate oxide layer form an interface therebetween, and said passivating substance X is also present at said interface between said channel region and said gate oxide layer, with a formation of Si-X bonds.

6 (withdrawn). The semiconductor configuration according to claim 3, wherein:

the MOSFET is one of a plurality of MOSFETs of the semiconductor configuration; and

mutually adjacent MOSFETs are isolated from one another by Mesa insulation.

7-15 (cancelled).

16 (previously presented). A method of fabricating a semiconductor configuration, which comprises the following steps:

fabricating a semiconductor structure having a base layer, an insulation layer, a monocrystalline silicon layer, and an interface between the insulation layer and the monocrystalline silicon layer;

placing a passivating substance X into the monocrystalline silicon layer, during or after the fabrication of the semiconductor structure; and

heat-treating the semiconductor structure with the passivating substance X for causing the passivating substance X in the monocrystalline silicon layer to diffuse both to the interface and to a surface of the monocrystalline silicon layer opposite to the interface.

17 (previously presented). The method according to claim 16, wherein the introducing step comprises ion-implanting the passivating substance X.

18 (currently amended). The method according to claim 17, wherein the introducing step is performed such that there is an implantation concentration maximum for the passivating substance X in the vicinity of the interface.

19 (previously presented). The method according to claim 16, wherein the fabricating of the semiconductor structure comprises the following steps:

providing two silicon semiconductor substrates;

oxidizing and forming a respective oxide layer on the two silicon semiconductor substrates;

joining the two silicon semiconductor substrates by contacting the two oxide layers; and

partially removing one of the silicon semiconductor substrates and forming the monocrystalline silicon layer.

20 (previously presented). The method according to claim 16, which comprises forming a covering oxide layer on the monocrystalline silicon layer.

21 (previously presented). The method according to claim 16, which comprises patterning the monocrystalline silicon layer by etching away regions thereof down to the underlying insulation layer.

22 (previously presented). The method according to claim 21, wherein the patterning step is performed before the step of

introducing the passivating substance X into one of an insulation layer and the monocrystalline silicon layer.

23 (previously presented). The method according to claim 21, wherein the patterning step is performed after the step of introducing the passivating substance X into one of the insulation layer and the monocrystalline silicon layer.

24 (previously presented). The method according to claim 16, which comprises:

doping the monocrystalline silicon layer differently region by region by ion implantation; and

performing the doping step after the step of introducing the passivating substance X and the heat-treating step.

25 (previously presented). The method according to claim 21, wherein the step of introducing a passivating substance X into the monocrystalline silicon layer is performed such that an implanted dose of the passivating substance X is below an amorphizing dose of silicon.